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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,289	12/21/2001	Sergio Tommaso Spampinato	853063.497	4035

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EXAMINER

FARAHANI, DANA

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/032,289

Applicant(s)

SPAMPINATO, SERGIO  
TOMMASO

Examiner

Dana Farahani

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 December 2003.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14, 23-26 and 31-44 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14, 23-26 and 31-44 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All   b) ☐ Some \*   c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 38 recites the limitation "the first zone" and "the second zone " in the last four lines. There is insufficient antecedent basis for this limitation in the claim.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-4, 6-14, 23-26, 31, 32, and 34-43 are rejected under 35 U.S.C. 103(a) as being anticipated by Aiello et al., hereinafter Aiello (U.S. Patent 6,127,723), in view of Yi et al., hereinafter Yi (U.S. Patent 6,207,481), all previously cited

Regarding claims 1, 6-8, 14, and 31, Aiello discloses in figure 2a an Integrated device being integrated in a chip of semiconductor material 218 of a first conductivity type, said chip having a first (lower) surface and a second (upper) surface opposite to each other, said device comprising a first transistor Td1 having a base region (242), an emitter region (251) and a collector region; a second transistor (comprising regions 218, 209, and 206 ) which is connected with the first transistor; a quenching element (pn junction of 242 and 218) of the first transistor, which discharges current there from when

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said second transistor is turned off, said quenching element being coupled with the base terminal of the first transistor and with the other not drivable terminal of the second transistor, said quenching element having at least one Zener diode, said at least one Zener diode being formed on the second surface of said chip and comprising a layer having at least one zone of the first conductivity type and at least one zone of a second conductivity type in order to form at least one P-N junction.

Aiello does not disclose the zener diode is a polysilicon.

Yi discloses a transistor, wherein it teaches using polysilicon results in uniform crystal size and a better transistor performance. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use polysilicon in Aiello's structure, as Yi teaches, since using polysilicon is advantageous, as mentioned above.

Regarding claim 2, the chip comprises a first region 242 of the second conductivity type which extends from the second surface into the chip and a second region 251 of the first conductivity type which extends from the second surface into the first region, and the first region, the second region and a portion of the chip comprised between the first region and the first surface forming respectively the base region, the emitter region and the collector region of the first transistor.

Regarding claim 3, the first transistor and said second transistor are bipolar transistors and said chip comprises a third region 209 of the second conductivity type which extends from the second surface into the second region and a fourth region 218 of the first conductivity type which extends from the second surface into the third region,

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each of the first region, of the third region and of the fourth region forming respectively the collector region, the base region and the emitter region of the second transistor.

Regarding claims 4 and 40, a third bipolar transistor Td2 connected with the first transistor in a Darlington configuration and the collector terminal of the first transistor is connected with the collector terminal of the third transistor.

Regarding claims 9-12, 41, and 42, the at least one polysilicon Zener diode comprises first and second polysilicon Zener diodes (one comprises regions 242 and 218; and the other is 209 and 206. Similarly, there are plurality of diodes corresponding to regions 239, 242 and 245) in back to back connection wherein the anode of the first Zener diode is connected with the anode of the second Zener diode and the cathode of the first Zener diode is connected with the base terminal of the first transistor and the cathode of the second Zener diode is connected with said other not drivable terminal of the second transistor.

Regarding claim 13, region 257 of figure 2a is an insulating layer (see column 3, line 50).

Regarding claims 23-26, 32, and 43, Aiello discloses the limitations in the claims, as above discussed, further disclosing insulating layer 257 and polysilicon layer 218 on the insulating layer.

Regarding claims 5 and 39, Aiello discloses in figure 4a MOS transistor Me, third and fourth regions 410 and 420, respectively. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make a MOS transistor in

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the embodiment of figure 2a in order to make the emitting-switching structure of figure 4b.

Regarding claim 34, Aiello discloses in figure 2a, a chip of semiconductor material, the chip having a first surface and a second surface opposite to each other, the device comprising a first transistor, Td1, having a control region 242 and first and second conduction regions, 251 and the region directly below region 242, respectively, a second transistor, Td2, having a control region 245 and first and second conduction regions, 254 and the region directly below region 245, respectively, the first conduction region of the second transistor being connected to the second conduction region of the first transistor, as can be seen in the figure; and quenching means D1, the quenching means being connected between the control terminal of the first transistor and the second conduction region of the second transistor, and including a first zone of the first conductivity type and a second zone of a second conductivity type in order to form a first P-N junction, shown in the figure.

Regarding claim 35, Aiello discloses in figure 2a the control region of the second transistor includes a first region 242 of the second conductivity type that extends from the second surface (top) into the chip, the second conduction region of the second transistor includes a second region 218 of the first conductivity type the extends from the second surface into the first region, and the first conduction region of the second transistor includes a third region 254 of the first conductivity type positioned between the first region and the first surface.

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Regarding claim 36, the first transistor and the second transistor in figure 2a are bipolar transistors, the second conduction region (218) of the first transistor includes the third region (254), the first conduction terminal 251 of the first transistor includes a portion of the chip between the third region and the first surface, as can be seen in the figure, and the control region 242 of the first transistor includes a fourth region 242 positioned between the third region 254 and the portion of the chip between the third region and the first surface, as can be seen in the figure.

Regarding claim 37, note that a first transistor also could have been consisted of regions 218, 209 (second buried region) and 215 (first buried region), wherein the second conduction region is 218, and the transistor control region are regions 209 and 221. In this case, Td1 is the second transistor, and Td2 is the third transistor.

Regarding claim 38, the second conduction region 218 of the second transistor includes a region 236 of the first conductivity type extending from the top surface into the chip, the device further comprising a sinker region 221 that extends from the second surface, or top surface of the chip into the second buried region 209.

5. Claims 33 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aiello in view of Yi as applied to claim 1 above, and further in view of Kato et al., hereinafter Kato (US Patent 4,994,880).

Aiello in view of Yi renders obvious the claimed invention, as discussed above, except for the emitter region of the first transistor extends as a comb shape.

Kato discloses in figure 8A, emitter surface electrode 47 is in a comb shape. Therefore, it would have been obvious to one of ordinary skill in the art at the time the

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invention was made to use a comb shape emitter in order to save space on the semiconductor chip.

***Response to Arguments***

6. Applicant's arguments filed on 12/9/03 have been fully considered but they are not persuasive.

Applicant argues that there is no motivation to combine the primary and the secondary reference. Note that the Yi reference is merely cited to show the obviousness of interchanging a monocrystalline material with a polycrystalline one. The Yi reference has not been structurally combined in any way with the primary reference, and it is cited to show that it is within the level of ordinary skill in the art to use either a polycrystalline or a monocrystalline material. Furthermore, case laws make it clear that choosing an appropriate material is in fact within the level of ordinary skill in the art.

Applicant further argues that the limitation in claim 1, namely, the diode is connected with the base region of the first transistor and with the not drivable terminal of the second transistor is not in the references. As discussed in the above rejections, diode D1 has such connections to transistors Td1 and Td2 (or, alternatively, Td1, and the transistor comprising regions 218, 209 and 215). See figure 2b, Also.



***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on M-F 9:00AM - 6:00PM.

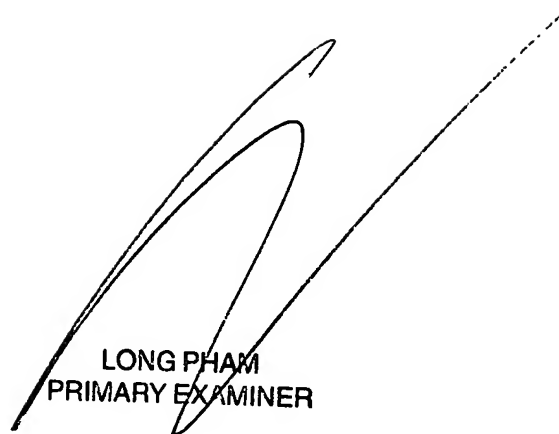
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (703)308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9318 for regular communications and (703)872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

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Dana Farahani  
March 27, 2004



LONG PHAM  
PRIMARY EXAMINER